

CLAIMS

What is claimed is:

1. Method for testing an integrated circuit (IC) which has at least one signal output (OUT)
5 and can be switched into a test mode and which has at least one circuit unit (SCH),
wherein
 - a potential value is applied at the signal output (OUT) in order to switch into the test mode, and
 - in the test mode a test signal (SW1, SW2) generated by the circuit unit (SCH) is applied
10 at the signal output (OUT).
2. Method in the test mode, according to claim 1, **wherein** the potential value at the signal output (OUT) is generated by means of a passive component, for example a resistor (W1, W2).
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3. Method according to claim 1 **wherein**, in the test mode, the circuit unit generates a plurality of test signals (SW1, SW2) which in each case are sent to the signal output (OUT) by applying specific potential values.
- 20 4. Method according to claim 2 **wherein**, in the test mode, the circuit unit generates a plurality of test signals (SW1, SW2) which in each case are sent to the signal output (OUT) by applying specific potential values.
- 25 5. Method according to claim 4 **wherein** the potential at the signal output (OUT) is compared with a defined reference value (P1, P2, P3, P4) within a first defined time window, and the integrated circuit (IC) is switched into the test mode in a second time window.
- 30 6. Method according to claim 5 **wherein** the potential value is applied at the signal output (OUT) and the test signal (SW1, SW2) is output at another signal output.
- 35 7. Method according to claim 5 **wherein** the switchover into the test mode is a function of the result of a logical operation, and the logical operation is made between the potential value applied at the signal output (OUT) and a signal (OS) generated by the circuit component (SCH).
8. Method according to claim 2 **wherein** circuit blocks within the circuit unit (SCH) are activated or deactivated with the switchover into the test mode.

9. Method according to claim 7 **wherein** circuit blocks within the circuit unit (SCH) are activated or deactivated with the switchover into the test mode.
- 5 10. Method according to claim 2 **wherein** the potential value applied at the signal output (OUT) lies within an interval of a window discriminator.
11. Method according to claim 9 **wherein** the potential value applied at the signal output (OUT) lies within an interval of a window discriminator.
- 10 12. Method according to claim 10 **wherein** the signal value of the test signal (SW1, SW2) lies within the voltage interval defined by the window discriminator.
13. Method according to claim 12 **wherein** the signal value of the test signal (SW1, SW2) lies within the voltage interval defined by the window discriminator.
- 15 14. Circuit arrangement for performing the method according to one of the claims 1 to 13 with an integrated circuit (IC) which has at least one signal output (OUT), at least one switching element (E1, E2) and at least one circuit unit (SCH),
wherein
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 - the integrated circuit (IC) has a control unit (ST) which is linked to the signal output (OUT) for testing the potential at the signal output (OUT), and
 - the control unit (ST) is linked to at least one switching element (E1, E2), and
 - the input of the switching element (E1, E2) is linked to an output of the circuit unit (SCH), and
 - the output of the switching element (E1, E2) is linked to the signal output (OUT).
- 25 15. Circuit arrangement according to claim 14,
wherein
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 - the control unit (ST) for adapting the signals to be tested to the potential of the signal output (OUT) contains an amplifier (LE1, LE2), and
 - the input of the amplifier (LE1, LE2) is linked to the output of a circuit unit (SCH1),
 - the output of the amplifier (LE1, LE2) is linked to the input of the switching element (E1, E2),
 - the control unit (ST) contains at least two comparators (I1, I2 and I3, I4) which form a window discriminator,
 - and has a logic gate (L1, L2) for performing a logic operation on the test signals (SW1, SW2) and at least one more signal (OS) of the circuit unit (SCH),
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- the input of the window discriminator is linked to the signal output (OUT), and
 - the output of the window discriminator is linked to the input of a logic gate (L1, L2),
 - the output of the logic gate (L1, L2) is linked to the control input of the switching element (E1, E2), and
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- the output of at least one logic gate (L1, L2) is also linked to the circuit unit (SCH1) for the selection of defined circuit elements within the circuit unit (SCH1).